

## PATENT ABSTRACTS OF JAPAN

(11)Publication number : 05-257164

(43)Date of publication of application : 08.10.1993

(51)Int.Cl.

G02F 1/136

G02F 1/1335

(21)Application number : 04-051817

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(22)Date of filing : 10.03.1992

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### (54) ACTIVE MATRIX SUBSTRATE

#### (57)Abstract:

**PURPOSE:** To suppress the generation of a signal delay by adopting the circuitry in which a light shielding film and additive capacity common wiring are connected in parallel.

**CONSTITUTION:** Metallic layers 10a to 10c are respectively so formed as to embed contact holes 7a to 7c and are connected to a source electrode, a drain electrode 24 and the additive capacity common wiring 8. The light shielding film 15 is so patterned and formed as to embed the contact hole 9c in addition to the upper part of a thin-film transistor(TFT) 25. The light shielding film 15 constituted in such a manner and the additive capacity common wiring 8 are formed in parallel. The light shielding film 15 and the additive capacity common wiring 8 are electrically connected via the contact holes 7c, 9c respectively provided in first and second interlayer insulating films. Then, the circuitry in which the light shielding film 15 and the additive capacity common wiring 8 are connected in parallel is obtd. and the resistance is lowered, by which the generation of the signal delay is suppressed.

